WHAT IS CLAIMED IS:

1. An image filter circuit for generating unsharp image signals used to subject image signals to dodging treatment in an image processing apparatus for image processing the image signals, the image filter circuit comprising:

an IIR type filter for carrying out filtering treatment to generate the unsharp image signals; and

at least one FIFO type field memory for delaying image signals which are not subjected to the filtering treatment at said IIR filter for a time corresponding to the delay time of image signals which have been subjected to the filtering treatment at said IIR type filter.

2. An image filter circuit according to claim 1 wherein said IIR type filter is a low-pass filter, an all-pass filter, or the combination thereof.

3. An image filter circuit according to claim 1 wherein said at least one FIFO type field memory comprises more than one FIFO type field memories disposed in parallel, and writing of said image signals to one FIFO type field memory and reading-out of said image signals from other one FIFO type field memory are carried out sequentially in said more than one FIFO type memories.

4. An image filter circuit according to claim 1 further comprising a main controller for generating writing signals and reading-out signals of said at least one FIFO type field memory which control the operation timing of said at least one FIFO type field memory in accordance with the delay time of said image signals at said IIR type filter.

5. An image filter circuit according to claim 4 wherein said main controller comprises a first counter which counts the number of pixels in the horizontal and vertical directions of a reproduced image; a first flip-flop which generates said writing signals from the time period when said first counter starts counting the number of pixels in the horizontal and vertical directions of said reproduced image until the end of counting; a second counter which starts counting the number of horizontal and vertical delays of said image signals at said IIR type filter, as soon as said first counter starts counting; a third counter which starts counting the number of horizontal and vertical delays of said image signals at said IIR type filter, after said first counter finished counting; and a second flip-flop which generates said reading-out signals after said second counter finished counting the number of horizontal and vertical delays of said image signals at said IIR type filter, until the time period when said third counter finishes counting the number of horizontal and vertical delays of image signals at said IIR type filter.